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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/808,168	03/24/2004	Haowen Bu	TI 37782	4831

23494 7590 03/27/2006

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EXAMINER	
AHMADI, MOHSEN	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 03/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/808,168	BU ET AL.	
	Examiner	Art Unit	
	Mohsen Ahmadi	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *amendment of 03/06/2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) *11-13* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 14-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/09/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicants' response of 03/06/2006 has been entered in the record and considered. The final rejection is withdrawn in view of the applicants' amendment. Claims 11-13 have been withdrawn. Claims 1-10 and 14-23 have been examined under the new rejection as discussed below.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 9, 14, 15 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu (US Pat. 6,326,291).

The present claims generally require a method for manufacturing a semiconductor device, comprising: forming a protective layer over a polysilicon gate electrode located over a substrate to provide a capped polysilicon gate electrode; forming source/drain regions in substrate proximate capped polysilicon gate electrode; removing protective layer using an etchant; siliciding polysilicon gate electrode to form a silicided gate electrode; and siliciding source/drain regions. Claim 14, further requires the formation of an interconnection.

Regarding claims 1 and 14, Figure 2 of Yu discloses a semiconductor substrate 208 comprising a polysilicon gate electrode 212, and a capping layer 216 which is comprised of a hardmask material such as siliconoxynitride (SiON) which is disposed over the top of the polysilicon gate structure 212. Yu discloses a method of forming source 204 and drain 202 regions in the substrate proximate the capped polysilicon gate electrode. Yu discloses a method of removing protective layer using an etchant (See col 5, lines 43-44). Yu discloses a method of siliciding the polysilicon gate (silicidation metal) to form a silicided gate (See col 5, lines 60-63). Yu also discloses a method of siliciding source and drain regions that comprise of a metal silicide such as nickel silicide ($NiSi_2$) (See col 5, lines 16-18). Claim 14, further requires forming interconnects within dielectric layers located over substrate for electrically contacting semiconductor devices. Figure 10 and 11 of Yu, shows the formation of interconnect to the gate silicide. A second dielectric layer 250 is deposited over the gate silicide 240 and over the first dielectric layer 230. A gate interconnect 252 is formed on the second dielectric layer 250, and the gate interconnect 252 is conductively coupled to the gate silicide 240 with a gate via 254. In addition, a drain interconnect 256 is formed on the second dielectric layer 250, and the drain interconnect 256 is conductively coupled to the drain silicide 220 with a drain via 258. Similarly, a source interconnect 260 is formed on the second dielectric layer 250, and the source interconnect 260 is conductively coupled to the source silicided 222 with a source via 262 (See col 6 and 7, lines 61-67 and 1-9).

Yu, however, does not disclose siliciding source/drain region after siliciding polysilicon gate electrode. Yu, discloses forming the siliciding source/drain region before siliciding polysilicon gate electrode, however, it would have been obvious to one of ordinary skill in the art to change the sequence of process as disclose by Yu. See *In re Burhans*, 154 F.2d 690, 69 USPQ 330 (CCPA 1946).

Regarding claims 2 and 15, Figure 3 of Yu discloses a method of forming a silicide blocking layer over source and drain regions prior to siliciding polysilicon gate electrode. This dielectric layer 230 is comprised of a dielectric material such as silicon dioxide (SiO_2) (See col, 5 lines 25-30).

Regarding claims 9 and 22, Yu discloses in their invention the method of siliciding the source and drain regions, but do not discloses the method wherein the silicide extends under a portion of gate sidewall spacers.

However Yu discloses in the prior art the method where silicided source and drain regions 114 and 116 are extended under a portion of gate sidewall spacers 113 located adjacent to silicided gate electrode112. See figure 1.

It would have been obvious to one of ordinary skill in the art, at the time of invention, to form extending under a portion of gate sidewall spacers located adjacent silicided gate electrode because it is disclosed in the Yu et al reference as an unpreferred embodiment. Unpreferred embodiments must be considered in determining obviousness. See *In re Burckel*, 201 USPQ 67 (1979). Moreover, a reference is not limited to preferred embodiments. See *In re Boe* , 148 USPQ 507 (CCPA 1966). The

use of a structure disclosed in the prior art would be within the level of one of ordinary skill in the art.

Claims 3, 4, 5, 16, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu (US Pat. 6,326,291) in view of Chang (US Pat. 6,794,313).

Regarding claims 3, 4, 5, 16, 17 and 18, Yu discloses all of the claimed features as stated above except for growing a silicide blocking layer using a dry oxidation process and low temperature radical oxidation or plasma oxidation process, and the thickness of blocking layers.

Chang discloses an oxidation process to improve polysilicon sidewall roughness. Chang also discloses a new step for the creation of polysilicon gate electrode structure.

Regarding claims 3 and 16, Chang discloses a silicon dioxide layer which is formed over the surface of substrate, where the silicon dioxide, thermally grown in an oxygen-steam ambient at a temperature between 800 and 1,000 degrees C using a dry oxidation process (See col, 3 lines 48-53).

Regarding claims 4 and 17, Chang discloses a methods of oxidation that can be used for the creation of silicon dioxide in a dry oxygen and anhydrous hydrogen chloride in an atmospheric or low pressure environment or in a low temperature, high pressure environment and the like (See col, 3 lines 48-64).

Regarding claims 5 and 18, Chang discloses the thickness ranging for silicon dioxide, which are about 30 to 300 Angstrom (See col, 3 lines 53-54).

As Yu calls for the formation of silicon dioxide, it would have been obvious to one of ordinary skill in the art, at the time of invention, to use the method as disclosed by

Chang for forming the silicon dioxide layer. The selection of the reaction parameters for forming a silicon dioxide layer would have been *prima facie* obvious in view of the teaching of Chang.

Claims 6 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu (US Pat. 6,326,291) in view of Chan et al. (US Pat. 2005/0179098).

Regarding claims 6 and 19, Yu is relied upon as discussed above. Yu discloses the use of a hardmask layer such as siliconoxynitride as the protective layer.

However Yu does not discloses silicon nitride as the protective layer.

Chan et al. discloses a new method to form metal silicide gates in the fabrication of an integrated circuit device. The method comprises forming polysilicon lines overlying a substrate with a dielectric layer therebetween.

Chan et al. discloses a hard mask layer such as silicon nitride can be selectively etched with respect to the polysilicon gate, and is deposited by a CVD process to protect the top surface of the polysilicon gate (See page, 2 paragraph [0024]).

It would have been obvious to one of ordinary skill in the art, at the time of invention, to use a silicon nitride hardmask layer as disclosed by Chan et al. to protect the polysilicon gate as disclosed by Yu for their known benefit of protection of the underneath layer. Yu broadly calls for silicon oxynitride and other hardmask materials, and Chan discloses that silicon nitride is a known hardmask layer. Therefore, a *prima facie* case of obviousness is established.

Claims 7, 8, 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu (US Pat. 6,326,291) in view of Chan et al. (US Pat. 2005/0179098) further in view of Moore et al. (US Pat. 20010034129).

Yu and Chan et al. are relied upon as discussed above and discloses all of the claimed features as stated above except for the sidewall spacer including nitride, the different nitride composition of the spacer and the protective layer, and the nitride carbon content of 5-10%.

Furthermore, Chan et al. teaches nitride is a preferred insulating material for a gate sidewall and as Yu teaches any insulating material may be used.

Regarding claims 7 and 20, Chan et al. discloses the spacers comprise an insulator material, such as oxide or nitride. Preferably, the spacers comprise silicon nitride are formed adjacent capped polysilicon gate electrode (See page, 2 paragraph [0028]).

It would have been obvious to one of ordinary skill in the art, at the time of invention, to use the method of Chan et al. to form the spacer containing nitride because as Chan et al. teaches nitride is a preferred insulating material for a gate sidewall and as Yu teaches any insulating material may be used. Furthermore it has been held that the selection of a known material based on its suitability for its intended use supported a *prima facie* obviousness determination in Sinclair & Carroll Co. v. interchemical Corp., 325 U.S. 327,65 USPQ 297 (1945). See also In re Leshin, 227 F.2d 197, 125 USPQ 416 (CCPA 1960).

Regarding claims 8 and 21, Yu discloses all of the claimed features as stated above except for the nitride layer has from about 5% to about 10% carbon content.

Moore et al. discloses a capacitor constructions, DRAM construction, semiconductive material assemblies, etching process, and methods for forming capacitors and DRAMs.

Moore et al. discloses an etch stop layer for example silicon nitride to form the substrate where silicon nitride layer having from 2% to about 20% carbon incorporated (by weight) (See page, 4 paragraph [0045]).

It would have been obvious to one of ordinary skill in the art, at the time of invention, to use nitride layer that has about 5% to about 10% carbon content as disclosed by Moore et al. to form the sidewall spacer containing nitride as disclosed by Yu and Chan et al. for their known benefit selectivity when etching for integration or interconnects (See page, 4 paragraph [0046]). It also has been held that the selection of a known material based on its suitability for its intended use supported a *prima facie* obviousness determination in Sinclair & Carroll Co. v. interchemical Corp., 325 U.S. 327,65 USPQ 297 (1945). See also In re Leshin, 227 F.2d 197, 125 USPQ 416 (CCPA 1960). Moreover, the formation of the spacer using the nitride of Moore et al. would result in a different chemical composition than the nitride which is used as the blocking layer as disclosed by Yu and Chan et al. as Chan et al. does not specify the carbon content of its nitride layer.

Claims 10 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu (US Pat. 6,326,291) in view of Chan et al. (US Pat. 2005/0179098).

Regarding claims 10 and 23, Yu discloses all of the claimed features as stated above except for the thickness of protective layer.

Chan et al. discloses a method where the protective layer, silicon nitride has a thickness ranging from about 100 angstroms to about 1,000 angstroms (See page, 2 paragraph [0024]).

It would have been obvious to one of ordinary skill in the art, at the time of invention, to use the thickness ranges as disclosed by Chan et al. in the protective layer as disclosed by Yu for their known benefit in protecting silicide layers. The examiner notes both references are drawn to analogous art, the protection of silicide layers using hard mask nitride and therefore a *prima facie* cases of obviousness is established.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mohsen Ahmadi whose telephone number is 1-571-272-5062. The examiner can normally be reached on Mon-Fri 8:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 1-571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MA Mahmoud Ahmadi
03/14/2006

3/17/06
Primary Examiner
Au 2812